

- 20 -

Claims

1. A method for synchronization adaptation of asynchronous
5 digital data streams comprising the steps of
 providing a first digital data stream (PCM_IN) at a
 first sample rate (CLK_1);
 inputting said first digital data stream (PCM_IN) to a
 sample rate conversion means (SRC);
10 supplying data output from said sample rate conversion
 means (SRC) to a processing element (BUFFER);
 storing said supplied data into said processing
 element (BUFFER); and
 outputting said data stored in said processing element
15 as a second digital data stream (PCM_OUT) at a second
 sample rate (CLK_2), with said first and said second sample
 rates (CLK_1, CLK_2) being different from each other;
 characterized by the further steps of
 detecting a state (BUFFER_STATUS) of said processing
20 element (BUFFER); and
 controlling said sample rate conversion means (SRC)
 dependent on the detected state of said processing element.
2. A method for synchronization adaptation of asynchronous
25 digital data streams according to claim 1,
 characterized in that
 said state (BUFFER_STATUS) of said processing element
 (BUFFER) represents the amount of data currently stored in
 said processing element.
- 30 3. A method for synchronization adaptation of asynchronous
digital data streams according to claim 2,
 characterized in that
 said detection step comprises the steps of

- 21 -

comparing a current amount of data stored in said processing element with a lower limit (LL) and an upper limit (UL) of respective admissible data amounts stored in said processing element, and

5 setting said state (BUFFER_STATUS) of said processing element

 to a first value (FULL) in case the detected actual amount of stored data exceeds the upper limit (UL),

 to a second value (EMPTY) in case the detected
10 actual amount of stored data is below the lower limit (LL),
 and

 to a third value (OK) in case the detected actual amount of stored data is found to be between the lower limit (LL) and the upper limit (UL).

15

4. A method for synchronization adaptation of asynchronous digital data streams according to claim 3, characterized in that

 said controlling step controls said sample rate
20 conversion means to be enabled if said detected state (BUFFER_STATUS) has said first (FULL) or said second (EMPTY) value, and to be disabled if said detected state has said third value (OK).

25 5. A method for synchronization adaptation of asynchronous digital data streams according to claim 3 ~~or 4~~, characterized in that

 said controlling step comprises the steps of

 reducing the number of data samples contained in the
30 data output by said sample rate conversion means (SRC) and supplied to said processing means if said state has said first value (FULL),

 increasing the number of data samples contained in the data output by said sample rate conversion means (SRC) and

- 22 -

supplied to said processing means if said state has said second value (EMPTY), and

leaving the number of data samples contained in the data output by said sample rate conversion means (SRC) and
5 supplied to said processing means unchanged if said state has said third value (OK).

6. A method for synchronization adaptation of asynchronous digital data streams according to ~~any of the preceding~~

0 10 claim~~s~~ 1 ~~to~~ 5,

characterized in that

reducing and/or increasing the number of data samples contained in the data output by said sample rate conversion means (SRC) and supplied to said processing means is
15 randomized in time within the data stream, such that the position within the group where a sample is to be removed and/or to be added is randomly selected.

7. A device for synchronization adaptation of asynchronous digital data streams comprising
20

a sample rate conversion means (SRC) to which is input a first digital data stream (PCM_IN) at a first sample rate (CLK_1);

a processing element (BUFFER) for storing data output
25 from said sample rate conversion means (SRC), and for outputting said data stored in said processing element as a second digital data stream (PCM_OUT) at a second sample rate (CLK_2), with said first and said second sample rates (CLK_1, CLK_2) being different from each other;

30 characterized by

a detection means for detecting a state (BUFFER_STATUS) of said processing element (BUFFER); and

a control means for controlling said sample rate conversion means (SRC) dependent on the detected state of said processing element.

[illegible]